WHAT IS CLAIMED IS:

1. An intercommunicating apparatus for transmitting a plurality of intercommunicating signals parallel to one another from a first processor unit to a second processor unit of a duplex processor apparatus, said intercommunicating apparatus comprising:

an output driver connected to said first processor unit for transmitting said intercommunicating signals supplied from said first processor unit in the form of a serial signal having a redundancy data structure; and

an input driver connected to said output driver and said second processor unit for receiving said serial signal transmitted from said output driver to reproduce said intercommunicating signals in the form of parallel signals and to supply the reproduced intercommunicating signals to said second processor unit.

2. An intercommunicating apparatus as claimed in Claim 1, wherein said output driver comprises a coding circuit for producing an error detecting code signal as said serial signal, said input driver comprises an decoding circuit for decoding said error detecting code signal to detect an error on said error detecting code signal, said decoding circuit suspending supply of said reproduced intercommunicating signals to said second processor unit when said error is detected.

3. An intercommunicating apparatus as claimed in Claim 2, wherein said coding circuit comprises:

a redundancy bit producing circuit connected to said first processor unit for producing at least one redundancy bit on the basis of said intercommunicating signals, and

a multiplexing circuit connected to said redundancy bit producing circuit for multiplexing said intercommunicating signals and said redundancy bit(s) in a predetermined cycle to produce said serial signal,

said decoding circuit comprising:

a demultiplexing circuit connected to said multiplexing circuit for demultiplexing said serial signal into received intercommunicating signals and received redundancy bit(s),

a error detecting circuit connected to said demultiplexing circuit for detecting an error on said received intercommunicating signals by the use of said received redundancy bit(s), and

a signal holding circuit connected to said error detecting circuit and said second processor unit for holding said received intercommunicating signals to supply said received intercommunicating signals as said reproduced intercommunicating signals to said second processor unit.

4. An intercommunicating apparatus as claimed in Claim 3, wherein said error detecting circuit clears held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said error is detected.

5. An intercommunicating apparatus as claimed in Claim 3, said redundancy bit producing circuit comprises a parity generating circuit for generating a parity bit as said

redundancy bit.

6. An intercommunicating apparatus as claimed in Claim 3, said redundancy bit producing circuit uses an error correction code or a cyclic redundancy check code to produce said redundancy bit(s).

7. An intercommunicating apparatus as claimed in Claim 3, said cording circuit further comprises a timing generating circuit connected to said multiplexing circuit for generating a timing signal to decide said predetermined cycle.

8. An intercommunicating apparatus as claimed in Claim 3, said decoding circuit further comprises a timer circuit connected to demultiplexing circuit and said signal holding circuit for clearing held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said demultiplexing circuit does not receive said serial signal for a predetermined time period.

9. An intercommunicating apparatus as claimed in claim 1, said intercommunicating apparatus further comprises:

an additional output driver connected to said second processor unit and having the same structure as said output driver for transmitting additional intercommunicating signals supplied from said second processor unit; and

an additional input driver connected to said additional output driver and said first processor unit and having the same structure as said input driver for reproducing said additional intercommunicating signals to supply the reproduced additional intercommunicating signals to said first processor unit.

10. A method for transmitting a plurality of intercommunicating signals parallel to one another from a first processor unit to a second processor unit of a duplex processor apparatus, said method comprising the steps of:

changing said intercommunicating signals supplied from said first processor unit into a serial signal having a redundancy data structure;

reproducing said intercommunicating signals in the form of parallel signals from said serial signal; and

supplying the reproduced intercommunicating signals to said second processor unit.

11. A method as claimed in Claim 10, said serial signal comprising an error detecting code signal, said method further comprising the steps of:

detecting an error on said error detecting code signal, and

suspending supply of said reproduced intercommunicating signals to said second processor unit when said error is detected.

12. A method as claimed in Claim 10, wherein said changing step comprises the steps of:

producing at least one redundancy bit on the basis of said intercommunicating signals, and

multiplexing said intercommunicating signals and said redundancy bit(s) in a predetermined cycle to produce said serial signal,

said reproducing step comprising the steps of:

demultiplexing said serial signal into received

intercommunicating signals and received redundancy bit(s),

detecting an error on said received intercommunicating signals by the use of said received redundancy bit(s), and

holding said received intercommunicating signals in a signal holding circuit to supply said received intercommunicating signals as said reproduced intercommunicating signals to said second processor unit.

13. A method as claimed in Claim 12, wherein said reproducing step further comprises the step of:

clearing held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said error is detected.

14. A method as claimed in Claim 12, wherein said redundancy bit comprises a parity bit.

15. A method as claimed in Claim 12, wherein said redundancy bit(s) generated by use of an error correction code or a cyclic redundancy check code.

16. A method as claimed in Claim 12, wherein said changing step further comprises the step of:

generating a timing signal to decide said predetermined cycle.

17. A method as claimed in Claim 12, wherein said reproducing step further comprises the steps of:

clearing held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said serial signal is not received for a predetermined time period.